ECS Transactions, 41 (8) 163-176 (2011)
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Assessment of Durable SiC JFET Technology for +600 °C to -125 °C Integrated Circuit Operation

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Electrical characteristics and circuit design considerations for prototype 6H-SiC JFET integrated circuits (ICs) operating over the broad temperature range of -125 °C to +600 °C are described. Strategic implementation of circuits with transistors and resistors in the same 6H-SiC n-channel layer enabled ICs with nearly temperature-independent functionality to be achieved. The frequency performance of the circuits declined at temperatures increasingly below or above room temperature, roughly corresponding to the change in 6H-SiC n-channel resistance arising from incomplete carrier ionization at low temperature and decreased electron mobility at high temperature. In addition to very broad temperature functionality, these simple digital and analog demonstration integrated circuits successfully operated with little change in functional characteristics over the course of thousands of hours at 500 °C before experiencing interconnect-related failures. With appropriate further development, these initial results establish a new technology foundation for realizing durable 500 °C ICs for combustion engine sensing and control, deep-well drilling, and other harsh-environment applications.

Introduction

Extension of the operating temperature envelope of transistor-based integrated circuits (ICs) well above the effective 300 °C limit of silicon-on-insulator technology is expected to enable important improvements to aerospace, automotive, energy production, and other industrial systems (1-3). For example, extreme temperature ICs capable of 500 °C operation are considered vital to realizing improved sensing and control of turbine engine combustion leading to better fuel efficiency with significantly reduced pollution. The ability to place such ICs in engine hot-sections would beneficially eliminate extra wires and liquid cooling plumbing (i.e., extra weight and decreased reliability) that are required when using silicon ICs that are limited to operational temperatures well below 300 °C. In general, the competitive performance benefits to large systems enabled by extreme temperature ICs are recognized as quite substantial, even though most such systems require only a relatively small number of extreme temperature chips (1).

One critical requirement for all ICs, including extreme temperature ICs, is that they function reliably over a designed product lifetime. The emergence of wide bandgap semiconductors has facilitated semiconductor transistor and small IC demonstrations at extreme ambient temperatures of 500 °C or higher over the past two decades (4-15). However, most envisioned applications require reliable operation over long time periods at high temperature, on the order of thousands of hours or more. Without such long-term

durability, extreme temperature semiconductor ICs will not practically benefit (and will not be inserted into) the vast majority of important intended applications. Many previous reports of extreme temperature transistor or IC operation have focused on current-voltage (I-V) properties and gain-frequency performance with little or no mention of how long such parts operated at high temperature. Aside from work at the NASA Glenn Research Center (6, 14, 16-19), we are unaware of any published reports claiming semiconductor transistor operation for more than 100 hours at temperatures at or above 500 °C. In addition to extreme high temperature operating capability, some applications additionally require functionality at cold temperatures well below freezing, as might occur during engine cold-starts and deep-space transits.

Experimental

Circuit Technology

Driven by the primary need to realize integrated circuits with prolonged 500 °C operational durability, an epitaxial n-channel 6H-SiC junction field-effect transistor (JFET) IC technology baseline, shown in simplified cross-section on the left side of Fig. 1, was selected for development (19, 20). In particular, the epitaxial SiC pn-junction gate structure (with low operating gate current) is believed to be inherently more robust against high temperature degradation than other (insulated gate, Schottky gate, bipolar, heterojunction and/or III-N) transistor technology approaches that would otherwise (i.e., notwithstanding overriding durability consideration) offer frequency, power dissipation, and/or circuit design and performance benefits. Though it is non-planar, the mesa-etched epi-gate structure avoids defects and extreme activation temperatures associated with high-dose p-type implants in SiC (21-24). Despite inferior mobility compared to 4H-SiC, 6H-SiC was selected as having demonstrated superior polytype structural stability during some thermal processing steps (25-28). Even though SiC is known to be more chemically near-inert and diffusion resistant than silicon and III-V semiconductors, thermally activated degradation mechanisms at interfaces (such as metal-SiC, and/or SiC-insulator interfaces) or materials outside the semiconductor (such as metals, insulators, and/or packaging) have previously limited extreme temperature (i.e., ≥ 500 °C) stability/durability (1, 6, 9, 10, 14, 17). However, durable high temperature ohmic contacts to n-type SiC and high-temperature SiC packaging have both demonstrated prolonged 500 °C operational capability in oxidizing air atmosphere (29-35). The successful integration of these high temperature technologies into the epitaxial 6H-SiC JFET process is believed critical to the greatly prolonged 500 °C transistor and IC operation reported in this work.

Except where noted, the experimental procedures and packaged chip oven-test setup previously described in (16, 19) were employed. The integrated circuits were formed by patterning the top $TaSi_2$/Pt metal to interconnect depletion-mode 6H-SiC JFET's and n-type channel resistors on each chip. As demonstration of extreme temperature stability and durability were the primary goals of this work, no effort was made to optimize these simple demonstration integrated circuits for gain, frequency, power, or other usually relevant circuit performance metrics.

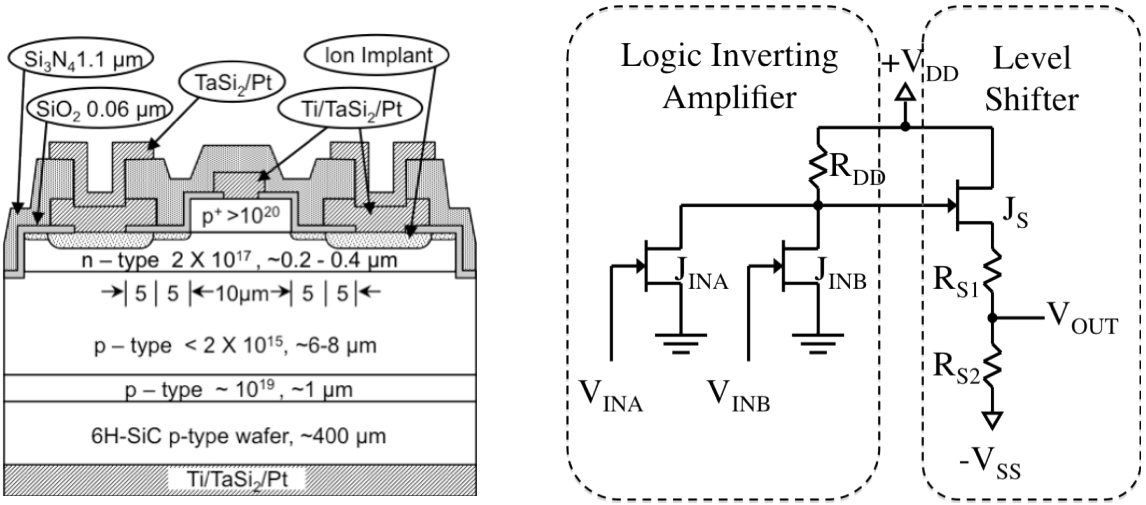

Figure 1. Simplified cross-sectional of 6H-SiC JFET (left) and schematic diagram of prototype 6H-SiC NOR logic gate (right) (19, 20, 36).

The circuit schematic of a demonstration two-input NOR logic gate that was implemented is shown on the right side of Fig. 1 (37, 38). The JFETs are depletion-mode ("normally-on") with significantly negative threshold voltages (that systematically varied from -14 V to -7 V across the wafer (20)). Therefore, this particular prototype logic family featured negative logic voltage levels and two power supplies with positive $+V_{DD}$ and negative $-V_{SS}$ in the range of 18 to 30 V. The negative logic levels ensure that input-stage (i.e., logic inverting amplifier stage denoted in Fig. 1) p^+ JFET gates J_{INA} and J_{INB} are reverse-biased (with low leakage current) with respect to JFET n-channels. Given sufficient JFET saturation current $I_{DSS} > V_{DD}/R_{DD}$, the input logic voltage signal drives the inverting amplifier stage output (drain node of J_{INA} and J_{INB}) to near $+V_{DD}$ (for $V_{IN} = V_{IL}$ = logic low input voltage) or near ground (for $V_{IN} = V_{IH}$ = logic high input voltage). This feeds a level-shifter stage (JFET J_S and resistors R_{S1} and R_{S2}) that translates the inverting amplifier output V_{OUT} back to desired negative logic gate output voltages (V_{OH} or V_{OL}) that would successfully drive the input of a subsequent gate of this logic family. To avoid forward-biasing the channel-to-substrate n-to-p junction diode, the p-type substrate is biased at $V_{Subs} = -V_{SS}$. This negative substrate bias slightly reduces the (negative) magnitude of JFET V_T and increases channel resistor values somewhat via substrate body bias effect (39, 40). Demonstration NAND gates were implemented by laying out J_{INA} and J_{INB} in series instead of parallel. It should be noted that the nominal implementation of this logic family, in which $R_{DD} = R_{S1} = R_{S2}$ and $|V_{SS}| = V_{DD}$ (37, 38), was not realized in the initial experiments.

Because of the time-dependent leakage phenomenon reported previously (20), electrical testing of the packaged circuits was initiated following more than 100 hours of unbiased "burn-in" soak at 500 °C. While three custom packaged logic gate chips have been tested over the full -125 °C to +600 °C temperature range to date, long term durability testing at 600 °C of circuits was not undertaken. Testing below room temperature was carried out using a commercially available cold chamber, while a commercial box oven was used for high temperature testing. Circuit output voltages were measured using 10 MΩ probes. NOR gates were packaged with access to the inverting amplifier stage output node so that the temperature-dependent characteristics of the inverting amplifier, its transistors (40μm gate width/10μm gate length J_{INA} in parallel

with 40μm/10μm J_{INB}), and drain resistor R_{DD} could be separately measured in addition to the overall logic gate input/output characteristics.

Inverting Amplifier

The resistive-load inverting amplifier is a fundamental sub-circuit of field-effect transistor integrated circuit technology. All other circuits described in this paper and our previous works (including differential amplifier stages and logic gates) contain similar transistor-resistor series sub-circuits and follow the same general temperature-dependent behavior trends (19). The inverting amplifier described in this section is actually a sub-circuit inside a packaged digital NOR gate. For the data presented in this section, the gates of J_{INA} and J_{INB} (each gate width 40 μm / gate length 10 μm, Fig. 1) were tied together to effectively form an 80μm/10μm JFET. The drain resistor R_{DD} for this particular circuit was formed from a 290 μm long by 15 μm wide (i.e., ~ 20 squares with end resistance) n-type 6H-SiC mesa resistor.

Nearly temperature-independent circuit behavior is desirable for a number of reasons, especially the fact that such behavior would simplify the interfacing and use of beneficial harsh-environment ICs in systems. Fig. 2 plots the inverting amplifier's JFET drain I-V characteristics (black solid lines) superimposed with the load resistor R_{DD} (grey dashed) "load line" I-Vs measured at (a) -123 °C, (b) +23 °C, and (c) +601 °C. To maintain consistency with substrate biases employed for integrated circuit operation (presented later), these I-V's were measured at a substrate bias V_{Subs} of -25 V. Aside from numerical current scale differences, the three Fig. 2 load line plots are qualitatively quite similar despite the extreme temperature differences. While a clear difference in JFET threshold voltage is evident between the -123 °C and +601 °C plots (by the number of steps it takes to turn off drain current I_D at each temperature), it is worth noting that the hot (+601 °C) and cold (-123 °C) load line I-Vs are quantitatively similar enough that they are plotted using the same current scale in Fig. 2(a) and 2(c). The I-V behavior exhibited in Fig. 2 is entirely consistent with previously reported temperature behavior of JFET and drain resistor parameters (36).

Despite the fact that transistor gain and current decrease more than 4-fold between room temperature and hot (+601 °C) or cold (-123 °C) temperature extremes, the inverting amplifier circuit voltage gain at low frequency is nearly temperature-independent. The measured inverting amplifier stage input voltage V_{IN} vs. output voltage V_{OUT} DC transfer characteristics at -125 °C, +23 °C, and +601 °C shown in Fig. 3(a) are quantitatively quite similar. Despite the large temperature difference, the high slope (i.e., high voltage gain) regions of the three transfer characteristics roughly parallel each other. However, there is significant shift in transfer curve position along the horizontal V_{IN} axis in the cold temperature characteristic that arises from the cold-temperature shift in JFET threshold voltage V_T. The fact that the maximum V_{OUT} in Fig. 3(a) is slightly less than V_{DD} = 30 V arises from "loading" current flowing through the 10 MΩ measurement probe to ground on the amplifier output that drops some voltage across R_{DD} even when the inverting amplifier JFET is turned off (for $V_{IN} < V_T$). This drop in V_{OUT} becomes more pronounced at the hot and cold temperature extremes as R_{DD} increases as a percentage of the constant (room-temperature) probe resistance.

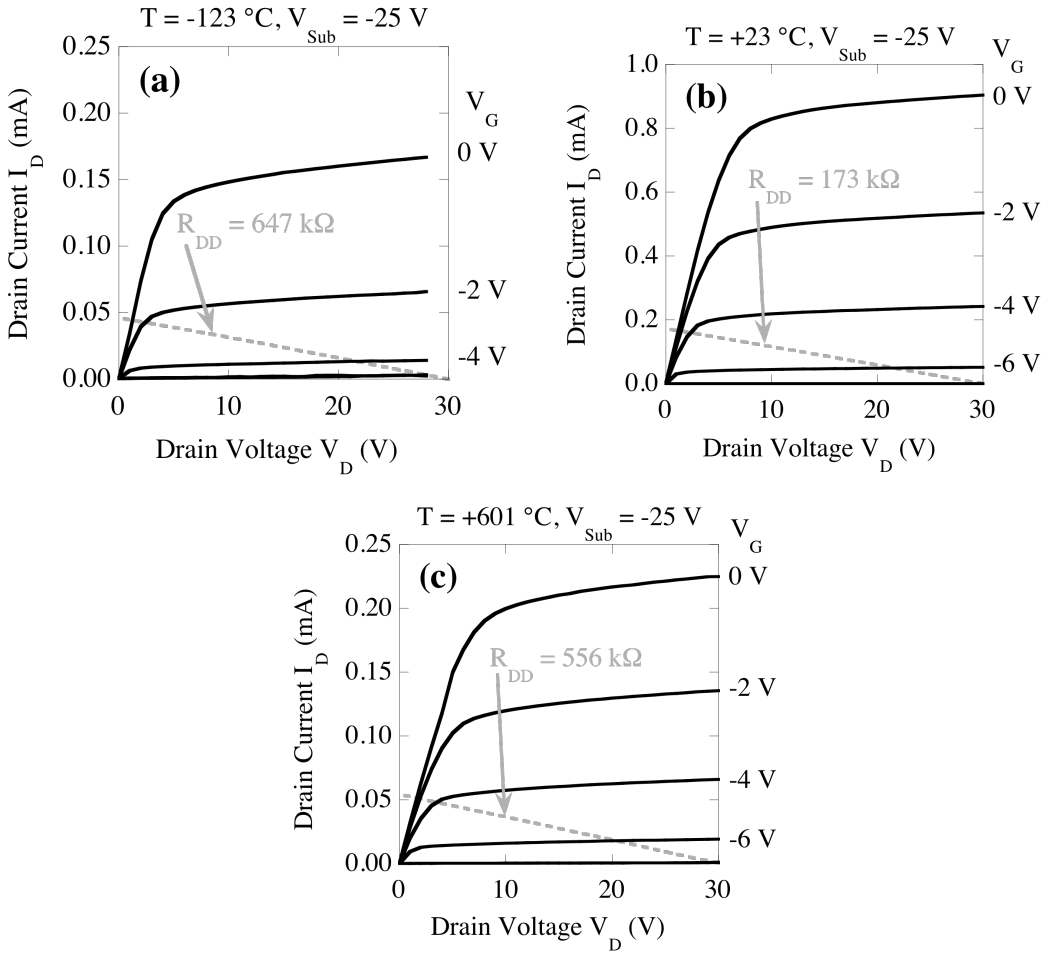

Figure 2. Current versus voltage "load line" characteristics of inverting amplifier stage measured at (a) -123 °C, (b) +23 °C, and (c) +601 °C. The characteristics of the 6H-SiC JFET (solid) and 6H-SiC epitaxial drain resistor R_{DD} (dashed grey) change nearly identically with changing temperature.

With proper selection of DC input bias to accommodate the somewhat shifting V_T, nearly temperature independent AC small signal voltage gain can be obtained. This occurs due to the fact that drain resistance R_{DD} increases with temperature at about the same rate that JFET transconductance gm and drain current I_D decrease, as previously described in (36). The key to this behavior is fact that the temperature dependence of these circuit-crucial parameters is dominated, oppositely, by the same temperature dependent conductivity parameters of the n-type 6H-SiC layer. In particular, g_m and I_D are directly proportional to the effective mobility and density of n-channel electrons (4, 8, 11-13, 41, 42), while 6H-SiC epitaxial resistor resistance R_{DD} is inversely proportional to these temperature-dependent channel electron parameters. This results in the circuit-critical R_{DD} x g_{m0} product being nearly constant over the entire temperature range (36). While this basic approach to circuit temperature stability is not new (see for example (43, 44)), this present work experimentally verifies its application to 6H-SiC JFET ICs operating over an extremely broad temperature range.

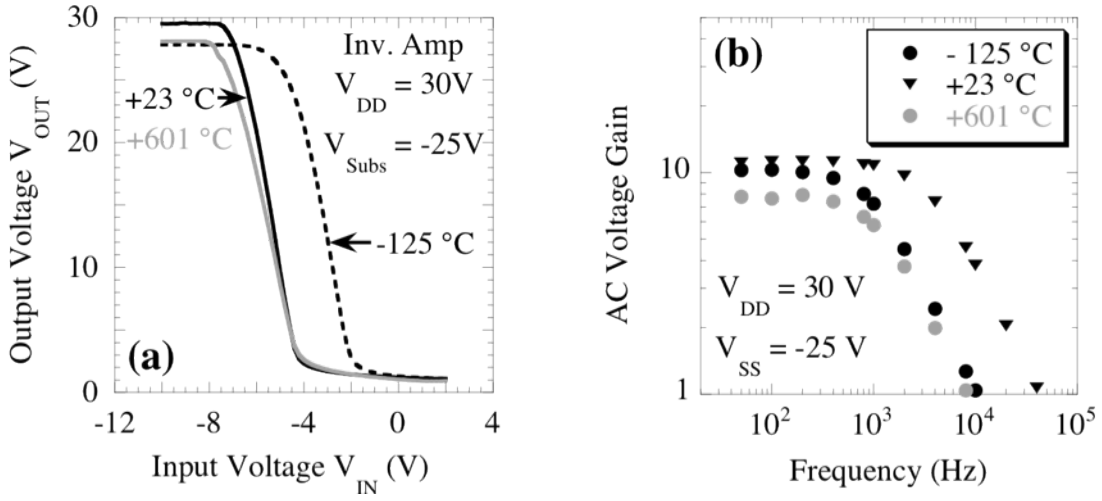

Figure 3. Experimentally measured gain-relevant properties of inverting amplifier stage measured at ambient temperatures of -125 °C, +23 °C, and +601 °C. (a) DC voltage transfer characteristics, and (b) AC amplifier voltage gain vs. frequency.

Our previous works have reported gain vs. frequency performance and quantitative temperature-dependent SPICE modeling of other inverting amplifier chips from this quarter-wafer for +25 °C < T < +500 °C (18, 19). Fig. 3b plots the experimentally measured NOR-gate inverting amplifier stage AC signal voltage gain as a function of test frequency at -125 °C, +23 °C, and +601 °C. To ensure operation in the high-gain region of the Fig. 3(a) transfer characteristics, the 500 mV amplitude AC test signal was superimposed on temperature-respective DC input biases of -3 V, -5 V, and -5 V. At low frequency AC signal voltage gains near 10 are observed at all three temperatures, in quantitative agreement with Fig. 3(a) transfer characteristics. It should be noted that the Fig. 3(b) frequency performance is inferior to our previous reports for other inverting amplifier chips (18, 19). However, this is attributed to higher (essentially temperature-independent) capacitance at the output node of this experimental setup that employed significantly more wiring and measurement circuitry (i.e., experimental setup that was not optimized for frequency response). Nevertheless, the Fig. 3(b) data shows that the amplifier's frequency performance degrades nearly 4-fold at the hot and cold temperature extremes relative to room temperature, in approximate agreement with the behavior of JFET n-channel conductance parameters (R_{DD}, R_{DS}, I_{DSS}, and g_m) as a function of temperature (36). With modest effort towards more optimized device layout, circuit design, and experiment parasitics, significantly higher 500 °C amplifier stage operating frequencies should be experimentally realized. Indeed, significantly higher frequency performance was achieved in subsequent tests (described below) of ring oscillator circuits that were conducted with reduced wiring and capacitance.

Logic Gate Integrated Circuits

Two-input NAND and NOR logic gate ICs experimentally demonstrated good functionality from -125 °C to +600 °C without any changes to power supply or input signal voltages. This broad operational temperature range is largely achieved via the same mechanisms described above for the inverting amplifier circuit. In particular, the logic gate output voltage for the Fig. 1 circuit is primarily determined by power supply

voltages (fixed) and ratios of JFET/resistor parameters that stay relatively constant as a function of temperature due to their joint dependence on SiC n-channel conduction properties.

Fig. 4 shows DC voltage transfer characteristics recorded from packaged (a) NOR and (b) NAND gate ICs measured near -125 °C, +23 °C, and +600 °C ambient temperatures. The NAND gate transfer characteristics are shifted right (to less negative values) nearly 3 V compared to the corresponding-temperature NOR gate transfer characteristics. This reflects the fact that these two chips were sawed from different regions of the quarter-wafer with somewhat disparate values for JFET threshold voltage V_T. Also, these two gates were implemented with different ratios of JFET gate width to resistor squares for both the logic inverting amplifier stage as well as the level shifter stage (Fig. 1). This necessitated the use of somewhat different power supply voltages and logic high and low test input signal levels between the two prototype gates, as indicated in Figs. 4 and 5. Once established however, the listed power supply voltages and test input signal levels were held fixed throughout all testing across the entire -125 °C to +600 °C temperature range.

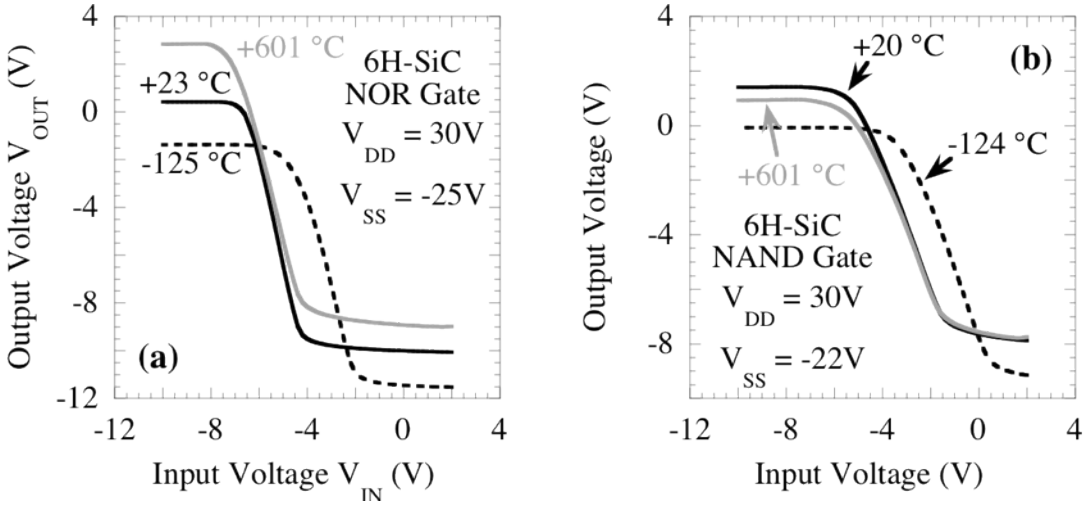

Figure 4. Plots comparing experimentally measured V_{OUT} versus V_{IN} DC transfer characteristics of packaged 6H-SiC JFET-based (a) NOR and (b) NAND logic gates near -125 °C, +23 °C, and +601 °C ambient temperatures.

Fig. 5 shows digitized input and output test waveforms measured from the (a) NOR and (b) NAND gate transient operational testing near -125 °C, +23 °C, and +600 °C ambient temperatures. For the entire temperature range, input and power supply voltage levels remained fixed at the levels displayed in Fig. 5. With sufficient settle time following input transitions, Fig. 5 logic output waveform levels are quantitatively consistent with corresponding Fig. 4 DC transfer characteristics. Fig. 6(a) plots NAND and NOR logic output voltages extracted from logic test waveforms after settling of transitions at all tested ambient temperatures. While some changes in logic low (V_{OL}) and logic high (V_{OH}) output voltages are observed, the gates demonstrate acceptable functionality with sufficient logic signal swing over the entire -125 °C to +600 °C measurement temperature range. In sharp contrast to output voltage behavior, the measured power consumption of the NAND and NOR gates plotted in Fig. 6(b) exhibits significant temperature dependence. This naturally arises due to the large change in

transistor and resistor current flow (Fig. 2) with temperature. The correlation of logic gate power dissipation with n-channel conduction properties is confirmed via comparison with the dashed line Fig. 6(b) plot of input JFET I_{DSS}.

The logic output transition times in Fig. 5 (i.e., output rise times and fall times) are observably longer for the extreme hot and cold temperatures than room temperature. Given that the gate outputs are directly driving long-wire and instrument-related capacitance, the output transitions in Fig. 5 do not accurately reflect inherent gate-to-gate signal propagation delay times.

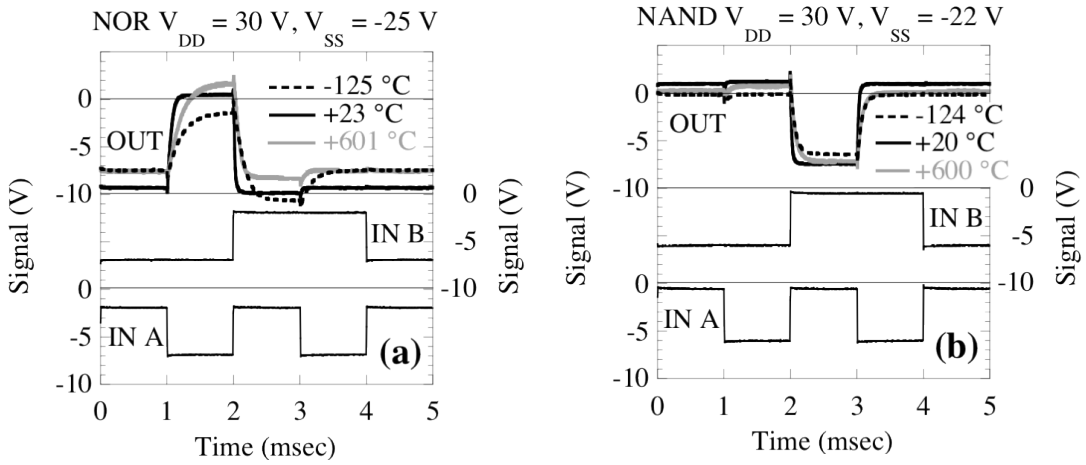

Figure 5. Digitized waveforms showing operation of packaged 6H-SiC JFET-based (a) NOR and (b) NAND logic gates at ambient temperatures near -125 °C, +23 °C, and +601 °C. The gates operated successfully across the entire temperature range without changing power supply or input signal voltage levels (see text).

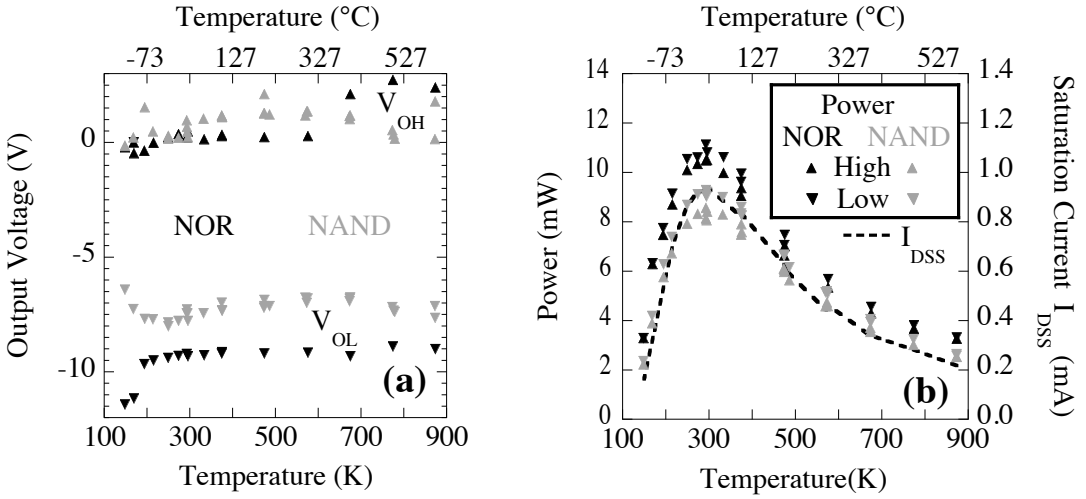

Figure 6. Experimentally measured NOR (black) and NAND (grey) (a) output voltage and (b) static-state power consumption plotted as a function of temperature. The output low (V_{OL}) and high (V_{OH}) voltage levels exhibit little change and sufficient swing across the measured temperature range. The static power exhibits large change as function of temperature that tracks the measured JFET I_{DSS} plotted as the dashed line in (b).

Ring Oscillator Circuits

Ring oscillator integrated circuits with output buffers are widely used to benchmark the switching speed of various digital logic IC approaches. Such completely integrated and buffered ring oscillator circuits are planned for future SiC JFET IC fabrication runs at NASA. In the meantime, we have constructed and characterized three different 3-stage ring oscillators with no output buffers by wiring inputs and outputs of separately packaged NOR and NAND gates into ring configuration. For one of these circuits (the slowest), the series input-to-output connections were made via long (> 50 cm) and unshielded wire bundles to the outside of the test chamber while for the other two (faster) circuits, the signal wiring took place with short (< 4 cm) wires directly connected to each other inside the test oven. All three gates in each of the respective three oscillator tests were tied to the same V_{DD} and V_{SS} power inputs, and an input/output node of each circuit was monitored via a longer gold wire running outside the oven to a 10 MΩ oscilloscope probe. Fig. 7 plots the measured oscillator frequencies (f_{OSC}) normalized to the room-temperature (peak) value as a function of ambient test temperature. For comparison, the normalized I_{DSS} measured from a NOR gate input JFET pair (normalized from same data set as shown in Fig. 6(b)) is also plotted in Fig. 7. The f_{OSC} temperature behavior tracks the JFET I_{DSS} behavior, confirming again that the 6H-SiC n-channel conduction physics dominates circuit frequency performance. In particular, charge supplied by the n-channel (resistor or transistor) current along with its total capacitance (including wiring) dictates the rate at which the measured output node voltage rises. Thus the oscillator test setup with substantially larger parasitic wiring capacitance exhibited substantially lower f_{OSC}.

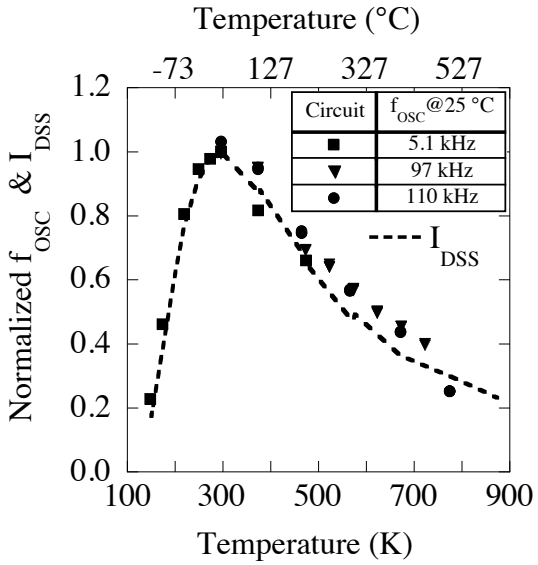

Figure 7. Ring oscillator frequency f_{OSC} temperature dependence measured from three different 3-stage ring oscillator circuits constructed from discrete NOR and NAND logic gates. The oscillation frequency exhibits large change as function of temperature that tracks the experimentally measured JFET I_{DSS} temperature behavior plotted as the dashed line. Both f_{OSC} and I_{DSS} are plotted normalized to their measured room-temperature values. Differences in experimental signal wiring capacitance (see text) are primarily responsible for the range in 25 °C f_{OSC} shown in the inset table.

Technology Assessment Discussion

Overall, chips from this quarter wafer have now yielded prototype semiconductor ICs with unprecedented stability and operational lifetime at 500 °C (16, 19, 20). Packaged analog amplifier stages and digital logic gate chips successfully operated in a laboratory oven for thousands of hours at 500 °C with little change in functional signal input/output characteristics. For example, Fig. 8 exhibits negligible difference between output voltage waveforms recorded from a NAND gate durability test measured in the 1st (black trace) and 2033rd (dashed grey trace) hour of 500 °C operational testing. This result was achieved with many of the test chips (and their interconnect metallization) directly exposed to oxidizing air ambient in lidless high temperature packages. As described in previous reports, IC failure usually occurred between 2000 and 5000 hours of 500 °C operational testing due to failure of interconnects running between transistors and resistors (19, 36). It is anticipated that future process improvements to passivate the interconnect metal will enable longer 500 °C IC durability.

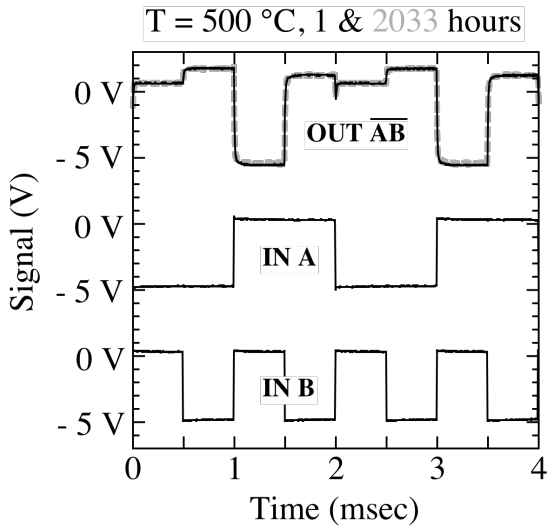

Figure 8. Operational test waveforms recorded from a packaged 6H-SiC NAND gate during the 1st (black trace) and 2033rd (dashed grey trace) hour of 500 °C operation.

As presented in the Experimental section, these prototype circuits also demonstrate nearly temperature-independent low-frequency signal voltage characteristics (without changes to input signals or power supply voltages) across the very broad -125 °C to +600 °C temperature range. Such temperature-independent circuit behavior is enabled by the fact that each circuit's 6H-SiC resistors and transistors share a common n-channel structure with common temperature-dependent conducting properties. The primary impact of increasing ambient temperature on circuit operation was decrease of maximum operating frequency. This frequency decrease with temperature corresponds to increasing n-channel resistance well known to arise from reduced channel electron mobility via increased thermal phonon scattering. The decreased current also correspondingly decreases circuit power dissipation at either temperature extreme.

Although only a small number of devices have been packaged and tested for thousands of hours at high temperature (19, 36), this demonstration establishes the initial feasibility of producing simple SiC integrated circuits that are capable of prolonged

500 °C operation. The increased 500 °C IC durability and stability demonstrated in this work is sufficient for sensor signal conditioning circuits in jet-engine ground test programs. Nevertheless, much further testing and validation of this technology is needed prior to actual insertion into most applications. Long-term testing of additional packaged devices, including testing under more aggressive and realistic environmental conditions (including thermal cycling, thermal shock, vibration at high temperature, etc.), is planned.

For many envisioned applications, far greater circuit complexity than the few-transistor ICs demonstrated in this initial work is required. Shrinkage of device dimensions and operating biases, and implementation of multilayer interconnects are obvious important further steps towards realizing durable 500 °C SiC integrated circuitry with greater complexity, higher frequency performance, and increased functionality. Processing to achieve shrinkage from the relatively large dimensions (10 μm gate lengths) used in this initial work appears relatively straightforward. However, such shrinkage will correspondingly increase current densities and electric fields in the operating chip. As such changes have often led to durability/reliability challenges throughout the development history of silicon-based ICs, it will naturally be important to accumulate similar fundamental understanding of scaling and reliability tradeoffs as extreme temperature SiC ICs are further developed.

Reduction of device power is also critical towards realizing increasingly complex integrated circuit functionality. The per-gate static power dissipation shown in Fig. 6(b) is many orders of magnitude larger than the static power dissipation logic gates implemented in silicon complementary metal oxide semiconductor (CMOS) ICs. This is largely due to the fact that significant current always flows through at least one branch of the circuit of Fig. 1 whereas a CMOS approach shuts off static-state current flow (39, 45). This fact precludes extreme temperature SiC JFET ICs from reaching the very high circuit complexity with low power dissipation that is common for room temperature silicon CMOS chips. If a SiC extreme temperature CMOS technology is ever developed in the future that exhibits prolonged (> 10,000 hours) durability/stability/reliability near 500 °C, that approach would inherently offer greater circuit functionality with lower power dissipation than is possible with SiC n-channel JFET IC technology. But the development of the necessary 500 °C long-term durable/stable/reliable CMOS-compatible gate insulator process appears to be a very daunting technical challenge that will probably require considerable time and effort to achieve. In the meantime, important long-term extreme temperature IC capability can be implemented with further development of durable SiC JFET IC technology. GaAs doped-channel FET IC experience suggests that SiC JFET IC circuit complexities in excess of 10^3-10^4 transistors per chip should be possible with technology optimization (46).

Acknowledgments

This work is presently funded by the NASA Aeronautics Research Mission Directorate in both the Aviation Safety and Fundamental Aeronautics Programs under the Vehicle Systems Safety Technologies, Subsonic Fixed Wing, and Supersonics Projects. Prior-year NASA funding for this work included the Glennan Microsystems Initiative, Ultra Efficient Engine Technology, Propulsion 21, Integrated Vehicle Health Management, and NASA Electronics Parts and Packaging programs. Work was carried out by the NASA Glenn Research Center. The process development and fabrication of the chips characterized in this communication was carried out primarily by D. Spry, G.

Behiem, C. Chang, R. Okojie, L. Evans, R. Meredith, and T. Ferrier. The high-temperature chip packaging was developed and implemented by L.-Y. Chen at NASA Glenn Research Center and Dr. Ender Savrun at Sienna Technologies, Inc. The authors are also grateful for the assistance of J. Flatico, D. Lucko, J. Jordan, K. Laster, J. Gonzalez, R. Lotenero, R. Buttler, M. Mrdenovich, B. Osborn, D. Androjna, A. Trunek, R. Patterson, A. Hammoud, G. Hunter, and L. Matus. Author P. Neudeck is grateful to C. D. H. Williams of MacSPICE.com for pointing him to the open-source SPICE that compiles on his computer and advice on SPICE MOSFET models.

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